UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,500	07/28/2003	Makoto Miyazawa	NEKU 20.544	5066

26304 7590 12/28/2005

KATTEN MUCHIN ROSENMAN LLP
575 MADISON AVENUE
NEW YORK, NY 10022-2585

EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,500	MIYAZAWA ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4-6* is/are allowed.

6)☒ Claim(s) *1,3 and 7-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The non-final rejection as set forth in paper No. (062405) is withdrawn in response to applicants' amendments. A new rejection is made as set forth in this Office Action. Claims (1 and 3-18) are pending in the application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, and 7-18 are rejected under 35 U.S.C. 103(a) as being obvious over Matsui (U.S. Patent 6,507,232) in view of Yusho (Japan Publication No. 2000-208707).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is

the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

In re claim 1, **Matsui** discloses a semiconductor integrated circuit device comprising: a terminal **100**; and a first capacitance adjusting section **103** which is connected to a wiring between the terminal and a protection resistor **101** in a front stage of an internal circuit **111** (col. 7, line 39 to col. 8, line 65 and FIGS. 3 and 4),

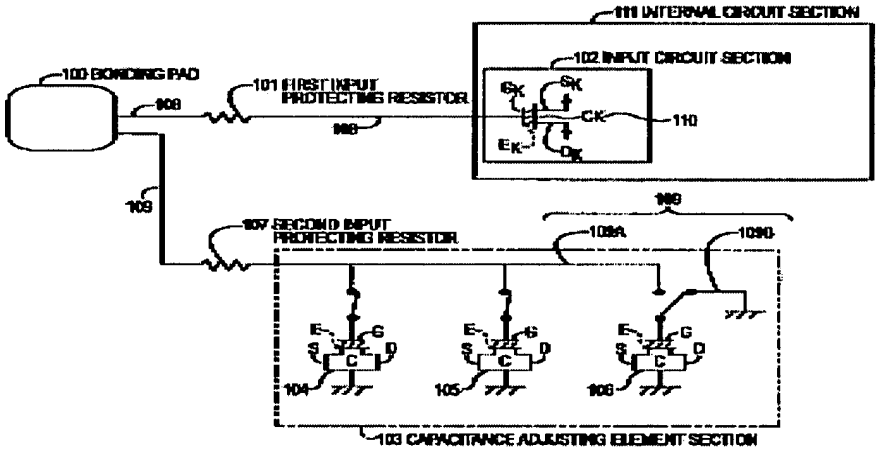
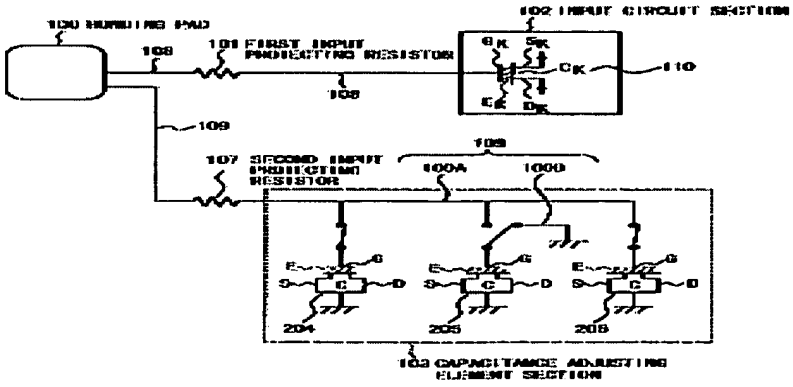


FIG. 3

Fig. 4

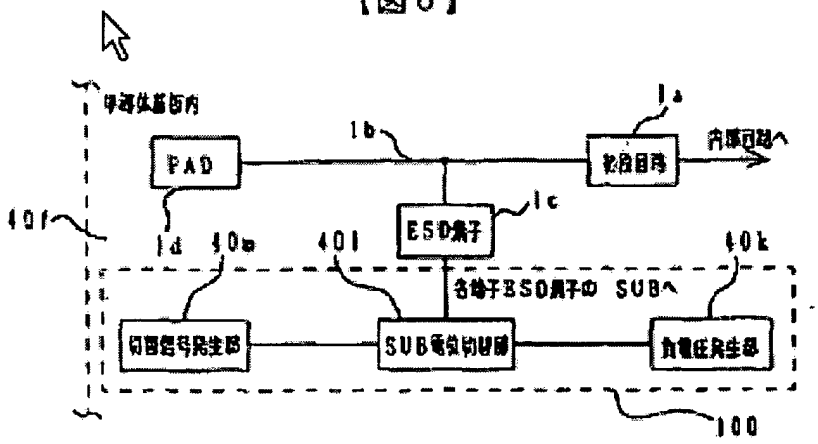


wherein the first capacitance adjusting section adjusts terminal capacitance of the terminal, based on capacitance of the first capacitance adjusting section (col. 7, line 39 to col. 8, line 65).

Matsui does not explicitly disclose that the semiconductor integrated circuit device according to Claim 1, further comprising: a protection circuit which is connected to the wiring between the terminal and the first capacitance section and protects the internal circuit.

Yusho, however, discloses a protection circuit (ESD) **1c**, which is connected **1b** to the wiring **20b** between the terminal (PAD) **1d** and the first capacitance section and protects the internal circuit (Patent Abstracts Of Japan and FIGS. 4 and 6 and related text).

【図６】



Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Matsui and Yusho to enable the protection circuit which is connected to wiring between the terminal and the first capacitance adjusting section of Matsui to be formed and furthermore to provide a

semiconductor device having a transistor for electrostatic protection is formed in the vicinity of a pad, and the terminal capacitance of the semiconductor device is made controllable (Abstract, Yusho).

In re claim 3, **Matsui** discloses a semiconductor integrated circuit device comprising: a terminal **100**; and a first capacitance adjusting section **103** which is connected to a wiring between the terminal and a protection resistor **101** in a front stage of an internal circuit **111** (col. 7, line 39 to col. 8, line 65 and FIGS. 3 and 4), wherein the first capacitance adjusting section adjusts terminal capacitance of the terminal, based on capacitance of the first capacitance adjusting section (col. 7, line 39 to col. 8, line 65), wherein the first capacitance adjusting section comprises a first adjusting capacitor which adjusts the terminal capacitance (col. 7, line 39 to col. 8, line 65 and FIG. 3), and wherein the first adjusting capacitor comprises: a first semiconductive portion which is composed of a first well region formed in a substrate with the internal circuit and having a conductive type opposite to that of the substrate, and a second semiconductive portion which is opposite to the first semiconductive portion and is composed of a first diffusion layer region formed in the first well region and having the same conductive type as that of the substrate (col. 7, line 62 to col. 8, line 39 and FIG. 4).

In re claim 7, **Matsui** discloses that the first capacitance adjusting section comprises a first adjusting capacitor which adjusts the terminal capacitance, the first adjusting capacitor comprises: a first semiconductive portion which is composed of a first well region formed in a substrate with the internal circuit and having a conductive type opposite to that of the substrate, and a second semiconductive portion which is opposite

to the first semiconductive portion and is composed of a first diffusion layer region formed in the first well region and having the same conductive type as that of the substrate (col. 7, line 62 to col. 8, line 39 and FIG. 4).

In re claim 8, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 7, further comprising: a well potential control section wherein the first capacitance adjusting section further comprises a second adjusting capacitor which adjusts the terminal capacitance based on controlling a well region potential by the well potential control section, the second adjusting capacitor comprises: a third semiconductive portion which is composed of a second well region formed in the substrate and having a conductive type opposite to that of the substrate, a fourth semiconductive portion which is opposite to the third semiconductive portion and is composed of a second diffusion layer region formed in the second well region and having the same conductive type as that of the substrate, and the well potential control section controls the well region potential of the second well region (col. 7, line 62 to col. 8, line 39 and FIG. 4).

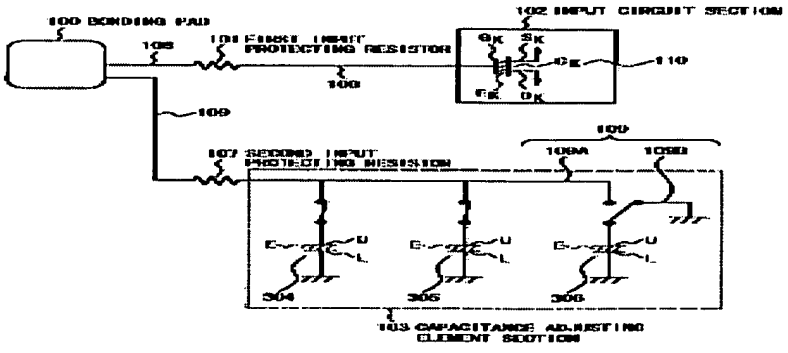
In re claim 9, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 8, wherein the well potential control section comprises: a plurality of resistors **101, 107** which are connected in series to each other between two potential electrodes; and a plurality of switches **104, 105, 106** each of which is connected in parallel to each of the plurality of resistors (FIG. 3),

the well potential control section controls the well region potential by controlling each one of the plurality of switches **104, 105, 106** (col. 7, line 66 to col. 8, line 29).

In re claim 10, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 9, further comprising: a plurality of the terminals **100**; and a plurality of the first capacitance adjusting sections **103** each of which is connected to each of a plurality of the wirings **108, 109** between each of the plurality of terminals **100** and each of a plurality of the protection resistors **101, 107**, wherein the well potential control section controls each of a plurality of said well region potentials (col. 7, line 39 to col. 8, line 65 and FIG. 3).

In re claim 11, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 1, further comprising: a second capacitance adjusting section which is connected to a wiring between the first capacitance adjusting section and the internal circuit, wherein the second capacitance, adjusting section adjusts the terminal capacitance based on capacitance of the second capacitance adjusting section; and a switching control section which controls the capacitance of the second capacitance adjusting section (FIG. 5).

Fig. 5



In re claim 12, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 11, wherein the switching control section comprises: a plurality of

switches **104, 105, 106** each of which outputs signal potentials corresponding to turn on and off of the each of plurality of switches, and a plurality of signal holding sections each of which holds corresponding each of a plurality of the signal potentials wherein the switching control section controls the capacitance of the second capacitance adjusting section based on the plurality of signal potentials (FIG. 4).

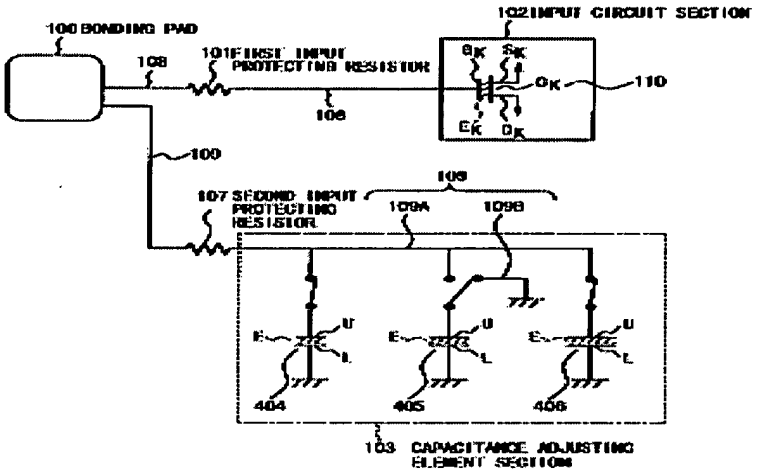
In re claim 13, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 12, wherein the second capacitance adjusting section comprises: a plurality of third adjusting capacitors each of which capacitance is variable based on corresponding each of the plurality of signal potentials, wherein the second capacitance adjusting section adjusts the plurality of third adjusting capacitors based on the plurality of signal potentials (FIG. 4).

In re claim 14, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 13, further comprising: a plurality of said terminals; and a plurality of the second capacitance adjusting sections each of which is connected to each of a plurality of the wirings between each of the plurality of the first capacitance adjusting sections and each of a plurality of the internal circuits, wherein the switching control section controls each of a plurality of said capacitances of the plurality of second capacitance adjusting sections (col. 4, line 54 to col. 11, line 10 and FIG. 6).

In re claim 15, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 3, further comprising: a second capacitance adjusting section which is connected to a wiring between said first capacitance adjusting section and said internal circuit, wherein the second capacitance adjusting section adjusts the terminal capacitance

based on capacitance of the second capacitance adjusting section; and a switching control section which controls said capacitance of said second capacitance adjusting section (col. 10, line 54 to col. 11, line 10 and FIG. 6).

Fig. 6



In re claim 16, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 15, wherein the switching control section comprises: a plurality of switches each of which outputs signal potentials corresponding to turn on and off of each of plurality of switches, and a plurality of signal holding sections each of which holds corresponding each of a plurality of said signal potentials, wherein the switching control section controls the capacitance of the second capacitance adjusting section based on the plurality of signal potentials (FIG. 6).

In re claim 17, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 16, wherein the second capacitance adjusting section comprises: a plurality of third adjusting capacitors each of which capacitance is variable based on corresponding the each of the plurality of signal potentials, wherein the second

capacitance adjusting section adjusts the plurality of third adjusting capacitors based on the signal potential (col. 10, line 54 to col. 11, line 10 and FIG. 6).

In re claim 18, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 17, further comprising: a plurality of said terminals; and a plurality of the second capacitance adjusting sections each of which is connected to each of a plurality of the wirings between each of the plurality of the first capacitance adjusting sections and each of a plurality of the internal circuits, wherein the switching control section controls each of a plurality of the capacitances of the plurality of second capacitance adjusting sections (col. 10, line 54 to col. 11, line 10 and FIG. 6).

Allowable Subject Matter

Claims 4-6 are allowed.

Response to Applicants' Amendment and Arguments

Applicants contend that the reference Matsui (U.S. Patent 6,507,232) herein known as Matsui does not show any distinct protection circuit, nor more particularly, a protection circuit connected to the wiring between the terminal and the first capacitance adjusting section.

In response to Applicants' contention that Matsui does not show any distinct protection circuit, nor more particularly, a protection circuit connected to the wiring between the terminal and the first capacitance adjusting section. Examiner respectfully submits that Applicants' argument is moot in view of the newly discovered reference to Yusho (Japan Publication No. 2000-208707) applied in this Office Action. Yusho discloses a protection circuit (ESD) **1c** which is connected **1b** to the wiring **20b** between

the terminal (PAD) **1d** and the first capacitance section and protects the internal circuit (Patent Abstracts Of Japan and FIGS. 4 and 6 and related text). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Matsui and Yusho to enable the protection circuit which is connected to wiring between the terminal and the first capacitance adjusting section of Matsui to be formed and furthermore to provide a semiconductor device having a transistor for electrostatic protection is formed in the vicinity of a pad, and the terminal capacitance of the semiconductor device is made controllable (Abstract, Yusho).

For this reason, Examiner holds the rejection proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
December 22, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER